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DOCKET NO. RBD-IC-2000				
PATENT APPLICATION TRANSMITTAL LETTER				
TO THE HONORABLE ASSISTANT COMMISSIONER OF PATENTS & TRADEMARKS:				
Transmitted herewith for filing is the patent application of: Robert Bruce DAVIES				
For: "DIE ATTACHMENT AND METHOD".				
Enclosed are:				
<input checked="" type="checkbox"/>	17 sheet(s) of drawings and 46 page(s) of specification			
<input checked="" type="checkbox"/>	A Declaration			
<input checked="" type="checkbox"/>	A Disclosure Statement and Cited Art			
<input checked="" type="checkbox"/>	A Verified Statement of Status as a Small Entity			
If a restriction of the claims is required, please examine first the group of claims including claim 1 and other analogous claim strings. This provisional election is only for the convenience of the USPTO and does not imply that a restriction is warranted, nor does it waive the right to traverse.				
CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
TOTAL CLAIMS	26-20	6	X \$9.00	\$54.00
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MULTIPLE DEPENDENT CLAIM(S)			\$120.00	
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TOTAL FILING FEE				\$438.00
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17 MAR 2000 DATE				
Robert B. Davies 433 E.MCKINLEY Tempe AZ 85281 (480) 945-4950				

STATEMENT OF SMALL ENTITY STATUS

Docket No. RBD-IC-2000

As the undersigned Applicant, I declare that I am entitled to pay reduced fees as a Small Entity under 37 CFR §1.27 for the invention for which a patent is sought before the Patent and Trademark Office entitled "DIE ATTACHMENT AND METHOD"

the specification of which (check one)

☒ is attached hereto.

☐ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I declare that I am entitled to pay reduced fees as a Small Entity because (check all that apply)

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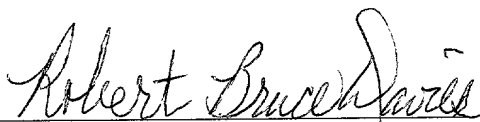
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Signature of Applicant or Authorized Officer

Date 17 MAR 2000

1 DIE ATTACHMENT AND METHOD

2
3 BACKGROUND OF THE INVENTION

4
5 Field of the Invention

6
7 This invention relates to a method of forming high
8 quality factor passive components on silicon substrates and
9 die attachment for die formed from silicon substrates.

10
11 More specifically, the present invention relates to
12 formation of a cavity beneath a dielectric platform formed
13 on a first surface of a silicon substrate.

14
15 In a further and more specific aspect, the present
16 invention relates to robust heatsinking of a silicon die
17 coupled with formation of high quality factor passive
18 components on the silicon die.

1 Prior Art

2

3 In operation of RF integrated circuits, it is
4 necessary to provide frequency-selective circuitry for
5 filtering signals, amplifying selected signals with respect
6 to other, unwanted signals and for other kinds of RF
7 functions. As frequencies increase, the provision of
8 frequency-selective components becomes more problematic,
9 especially in monolithic form.

10

11 Various kinds of frequency selection components have
12 been developed over the years. Some of these, such as
13 crystals and SAWs, depend on mechanical resonances to
14 provide frequency selectivity. These types of devices tend
15 to be incompatible with silicon circuitry requirements for
16 reasons having to do with materials engineering and also
17 because these types of devices require different, and much
18 more expensive, packaging than is typical for silicon
19 circuitry.

20

21 As a result, much work has focused on attempts to
22 provide LC frequency selection functions on silicon.
23 However, especially the inductors tend to be difficult to
24 form with high quality factor, also known as "Q".
25 Additionally, the kinds of inductors that have been made

1 tend to require large areas on the resulting integrated
2 circuit. Some systems opt for separately-packaged frequency
3 selection components, with the result that parts count is
4 increased.

5

6 In an article entitled "Integrated Passive Components
7 in MCM-Si Technology and their Applications in RF-Systems"
8 by J. Hartung, 1998 Intl. Conf. on Multichip Modules and
9 High Density Packaging, IEEE Cat. No. 0-7803-4850-8/98 (Aug.
10 '98), pp. 256-261, measured Qs and inductances for coils
11 fabricated on silicon multichip modules are presented. In
12 an article entitled "Applications for GaAs and Silicon
13 Integrated Circuits in Next Generation Wireless
14 Communication Systems" by L.M. Burns, IEEE JSSC, Vol. 30,
15 No. 10, Oct. 1996, pp.1088-1095, the demand for lightweight,
16 portable communications products is addressed through
17 monolithic integration of passive components in receivers
18 and transmitters. These articles address system-level
19 concerns that are met by combining separate circuits for the
20 frequency selection functions.

21 Monolithic integration of inductors is also addressed
22 in a variety of ways. For example, in an article entitled
23 "Analysis, Design, and Optimization of Spiral Inductors and

1 Transformers for Si RF IC's" by A.M. Niknejad and R.G.
2 Meyer, IEEE JSSC Vol. 33, No. 10, Oct. '98, pp. 1470-1481,

3 design rules are discussed and performance tradeoffs
4 are analyzed for spiral inductors.

5 In "A 1.8 GHz Low-Phase-Noise Spiral-LC CMOS VCO" by J.
6 Craninckx and M. Steyaert, IEEE Cat. No. 0-7803-3339-X 96
7 (1996), pp. 30-31, silicon and GaAs technologies are
8 discussed. Monolithic spiral inductors that are formed on
9 conductive substrates tend to have reduced Qs due to losses
10 that are caused by ground currents being induced in the
11 substrate beneath the spiral inductors.

12 Unfortunately, while GaAs substrates may be made to be
13 semi-insulating, thereby reducing or substantially
14 eliminating parasitic substrate currents, GaAs substrates
15 are expensive. Additionally, many GaAs devices have higher
16 standby power requirements than do silicon devices.

17 Silicon substrates are typically provided with a
18 lightly doped epitaxial layer for formation of active
19 components (e.g., transistors and the like). A more heavily
20 doped substrate is usually employed to support the epitaxial
21 layer and to provide a low resistance ground return path for

1 components formed in the epitaxial layer. Additionally, a
2 highly doped substrate aids in prevention of latch-up
3 phenomena.

4 While the heavily doped substrate provides a ground
5 return path for the active circuits, it also results in
6 reduced coil Q and losses when coils are formed on
7 insulating layers above the substrate. As a result, silicon
8 substrates that have been prepared for formation of active
9 components are poorly suited to formation of high Q
10 inductors.

11 One approach to providing monolithic inductors having
12 increased Q s is to form a thick dielectric layer on the
13 substrate. The inductors require a relatively thick
14 dielectric layer in order to be adequately isolated from the
15 conductive substrate. However, this results in a nonplanar
16 surface, which interferes with photolithographic processes
17 employed for definition of other circuit elements.
18 Additionally, these dielectric layers tend to result in
19 substantial stresses in the substrate, which can lead to
20 bowing of the substrate and other problems.

21 It would be highly advantageous, therefore, to remedy
22 the foregoing and other deficiencies inherent in the prior
23 art.

24

1 Accordingly, it is an object of the present invention
2 to provide improvements in masking for formation of high
3 quality, thick dielectric layers in silicon substrates.

4

5 Another object of the present invention is the
6 provision of an improved platform for formation of high
7 speed digital busses on silicon substrates.

8

9 An additional object of the instant invention is the
10 provision of an improved method and apparatus for providing
11 thick dielectric layers on silicon substrates while
12 preserving planarity of the substrate surface.

13

14 Moreover, an object of the instant invention is the
15 provision of an improved method and apparatus for providing
16 reduction in coil losses while preserving capability for
17 formation of active components on a silicon substrate.

18

19 Still a further additional object of the present
20 invention is to provide an improved process for forming
21 passive components on silicon.

22

23 Still another object of the present invention is the
24 provision of a method, system and apparatus for suppressing

1 losses in coils that are monolithically co-integrated with
2 other microelectronic components.

3

4 Yet still another object of the instant invention is
5 the provision of a method for forming thick, planar, low
6 dielectric constant, low loss dielectric layers in silicon
7 substrates.

8

9 And a further object of the invention is to provide a
10 method, system and apparatus for suppressing losses in
11 monolithic inductors.

12

13 And still a further object of the invention is the
14 provision of method and apparatus, according to the
15 foregoing, which is intended to improve operation of
16 inductors in monolithic silicon circuits.

SUMMARY OF THE INVENTION

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Briefly stated, to achieve the desired objects of the instant invention in accordance with an aspect thereof, provided is a semiconductor device including a die attach surface having a first pedestal and a first semiconductor die having a first surface formed with a first cavity for mounting the first semiconductor die on the first pedestal.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and further and more specific objects and advantages of the instant invention will become readily apparent to those skilled in the art from the following detailed description of preferred embodiments thereof taken in conjunction with the drawings in which:

FIG. 1 is a simplified plan view of a portion of an integrated circuit including an etch mask formed on a silicon substrate, in accordance with an embodiment of the instant invention;

FIG. 2 is a simplified and enlarged plan view of a portion of the dielectric platform shown in FIG. 1, in accordance with an embodiment of the instant invention;

FIG. 3 is a simplified side view, in section, taken along section lines 8-8 of FIG. 2, of a silicon substrate at another step in processing, in accordance with an embodiment of the present invention;

FIG. 4 is a simplified side view, in section, taken along section lines 8-8 of FIG. 2, of a silicon substrate at another step in processing, in accordance with an embodiment of the present invention;

1 FIG. 5 is a simplified side view, in section, taken
2 along section lines 8-8 of FIG. 2, of a silicon substrate at
3 another step in processing, in accordance with an embodiment
4 of the present invention;

5
6 FIG. 6 is a simplified side view, in section, taken
7 along section lines 8-8 of FIG. 2, of a silicon substrate at
8 another step in processing, in accordance with an embodiment
9 of the present invention;

10

11 FIG. 7 is a simplified and enlarged side view, in
12 section, taken along section lines 8-8 of FIG. 2, of a
13 silicon substrate at another step in processing, in
14 accordance with an embodiment of the instant invention;

15

16 FIG. 8 is a simplified side view, in section, taken
17 along section lines 8-8 of FIG. 2, of a silicon substrate at
18 another step in processing, in accordance with an embodiment
19 of the instant invention;

20

21 FIG. 9 is a simplified side view, in section, taken
22 along section lines 8-8 of FIG. 2, of a silicon substrate at
23 another step in processing, in accordance with an embodiment
24 of the instant invention;

25

1 FIG. 10 is a simplified and enlarged plan view of a
2 portion the dielectric platform shown in FIG. 1, in
3 accordance with an embodiment of the instant invention;
4

5 FIG. 11 is a simplified side view, in section, taken
6 along section lines 11-11 of FIG. 10, in accordance with an
7 embodiment of the instant invention;
8

9 FIG. 12 is a simplified plan view of a semiconductor
10 die including passive components, in accordance with an
11 embodiment of the instant invention;
12

13 FIGs. 13A-13E are simplified side views, in section,
14 taken along section lines 33-33 of FIG. 12, in accordance
15 with embodiments of the instant invention;
16

17 FIG. 14 is a simplified plan view of two
18 interconnected semiconductor die co-located on a common
19 mount, in accordance with embodiments of the instant
20 invention;
21

22 FIGs. 15A-15F are simplified side views, in section,
23 taken along section lines 35-35 of FIG. 14, in accordance
24 with embodiments of the instant invention.
25

1 FIG. 16 is a simplified side view of the die 80
2 portion of FIG. 15F, in accordance with embodiments of the
3 instant invention;

4

5 FIG. 17 is a simplified plan view of two
6 interconnected semiconductor die co-located and a
7 surrounding dielectric material ring on a common mount, in
8 accordance with embodiments of the instant invention;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Turning now to the drawings, in which like reference characters indicate corresponding elements throughout the several views, attention is first directed to FIG. 1, which illustrates a simplified plan view of an embodiment of a dielectric platform, generally designated by the reference character 12, in accordance with an embodiment of the instant invention.

FIG. 1 is a simplified plan view of a portion of an integrated circuit showing a dielectric platform 12 formed in a silicon substrate 10, in accordance with an embodiment of the instant invention. The substrate 10 includes one or more areas 11 that may be used to support active electrical components such as MOS and bipolar transistors, diodes, and the like. Active electronic components may be formed in the areas 11 using conventional CMOS, bipolar or BiCMOS processes. The dielectric platform 12 is outlined by a boundary 9 and the area 11 is outlined by a boundary 6. The dielectric platform 12 may be used to support passive electrical components such as interconnections, which may be formed from metals or doped polycrystalline silicon, for example.

1 The dielectric platform 12 may also be used to support
2 inductors, such as spiral inductors, or thin film resistors,
3 such as doped polycrystalline silicon or metal resistors.
4 The platform 12 may also be used to support capacitors
5 having two conductive plates separate by an insulating
6 dielectric. The conductive plates may each be formed from
7 metal, polycrystalline silicon or metal silicides. Examples
8 include metal-insulator-metal, poly-insulator-metal, metal
9 silicide-insulator-metal, poly-insulator-metal silicide or
10 poly-insulator-poly capacitors.

11
12 An advantage provided by the dielectric platform 12 is
13 that passive components formed on the dielectric platform 12
14 have greatly reduced capacitance to the conductive silicon
15 substrate 10. As a result, reduced amounts of electrical
16 power are required in order to switch electrical signals in
17 conductors and other components formed on the dielectric
18 platform 12, such as high speed digital busses and
19 interconnects.

20
21 Increased electrical Qs and increased operating
22 frequencies are possible for passive components formed on
23 the dielectric platform 12, as is discussed in the Annual
24 Report 1998 of the Institut für Halbleiter Physik (Prof. Abbas
25 Ourmazed, IHP 15230, pp. 50-51). The approach described in

1 this report provides improvements in coil Qs but also relies
2 on long trenches that are subsequently oxidized to provide a
3 thick dielectric having voids comprising only about 20% of
4 the total volume of the dielectric. Further, these
5 structures can result in substantial stresses being produced
6 in the directions of the trenches.

7
8 It will be appreciated that while only one of the
9 dielectric platforms 12 and areas 11 are shown in Fig. 1 for
10 simplicity of illustration and ease of understanding,
11 multiple examples of either may be formed on the substrate
12 10.

13
14 FIG. 2 is a simplified and enlarged plan view of a
15 portion of the dielectric platform 12 shown in FIG. 1, in
16 accordance with an embodiment of the instant invention.
17 Within the boundary 9 of region 12, a mask 13 is formed that
18 includes multiple openings 20. The openings 20 may have
19 any shape, however, hexagonal openings 20 are shown in FIG.
20 2. In one embodiment, the mask 13 is formed by oxidizing a
21 portion or all of the silicon substrate 10 followed by
22 conventional photolithography and etching. One or more
23 regions 7 may also be formed in portions of the mask 13.

24

1 In one embodiment, the openings 20 are formed to have
2 a width, measured along section line 8-8, of between 0.5 and
3 2 microns. In one embodiment, the openings 20 are formed to
4 have a width of about 1.2 microns and are separated by about
5 .4 microns.

6
7 FIG. 3 is a simplified side view, in section, taken
8 along section lines 8-8 of FIG. 2, of a silicon substrate 10
9 at another step in processing, in accordance with an
10 embodiment of the present invention. FIG. 3 illustrates a
11 mask layer 13 having openings 20 and cavities 21 formed by
12 etching the silicon substrate 10 through the mask 13. In
13 one embodiment, the cavities 21 are formed by conventional
14 anisotropic plasma etching of the silicon substrate 10 to
15 have a depth of between 1 and ten microns. In one
16 embodiment, the cavities are etched to have a depth of about
17 three microns. In one embodiment, the etching is carried
18 out using high speed anisotropic etching in a $\text{HBr/NF}_3/\text{He-O}_2$
19 plasma.

20 In one embodiment, the mask 13 is formed by
21 conventional oxidation of portions of the substrate 10,
22 followed by conventional photolithography and etching, such
23 as anisotropic plasma etching. In one embodiment, the mask
24 13 is formed to have a thickness of between 0.3 and 1.0

1 microns. In one embodiment, the mask 13 is formed to have a
2 thickness of about 0.6 microns.

3
4 FIG. 4 is a simplified side view, in section, taken
5 along section lines 8-8 of FIG. 2, of a silicon substrate 10
6 at another step in processing, in accordance with an
7 embodiment of the present invention. A conventional
8 isotropic etch of the silicon substrate 10 has been employed
9 to enlarge the cavities 21 and to reduce the thickness of
10 the sidewalls separating the cavities 21. In one
11 embodiment, the sidewalls are etched to have a thickness of
12 about .2 microns. In one embodiment, the sidewalls are
13 etched to have a thickness of between .1 and .4 microns.

14
15 FIG. 5 is a simplified side view, in section, taken
16 along section lines 8-8 of FIG. 2, of a silicon substrate 10
17 at another step in processing, in accordance with an
18 embodiment of the present invention. A conventional
19 oxidation has been employed to oxidize all exposed silicon
20 surfaces in the cavities 21, and the mask 13 has increased
21 in thickness to form a mask 14. In one embodiment, the
22 oxidation has been carried out to form an oxide layer 14.
23 In one embodiment, the sidewalls have been oxidized to
24 provide an oxide 14' having a thickness of between .01 and
25 .2 microns. In one embodiment, the sidewalls have been

1 oxidized to provide an oxide 14' having a thickness of about
2 .1 micron.

3
4 FIG. 6 is a simplified side view, in section, taken
5 along section lines 8-8 of FIG. 2, of a silicon substrate 10
6 at another step in processing, in accordance with an
7 embodiment of the present invention. A conventional
8 anisotropic plasma etch is used to remove the oxide layer
9 14' from bottoms of the cavities 21 but not from sidewalls
10 of the cavities 21.

11
12 A conventional silicon etch is used to remove silicon
13 from beneath the cavities 21 to provide one or more cavities
14 200. In one embodiment, the silicon etch is a high speed
15 plasma etch having predominantly anisotropic
16 characteristics. In one embodiment, alternating between
17 isotropic etching and anisotropic etching completes the
18 cavity 200. In one embodiment, one or more pillars 17 are
19 formed within the cavity 200 beneath the region 7. In one
20 embodiment, the cavity 200 is formed to have a depth of
21 between 2 and 15 microns, and the increase in width is
22 between .2 and .7 microns. In one embodiment, the cavity 200
23 is formed to have a depth of about 5 microns, and the

1 increase in width is about .5 microns. As a result of these
2 etches, a suspended lattice 18 comprised of silicon and a
3 silicon-based dielectric is formed above the cavity 200.

4
5 FIG. 7 is a simplified and enlarged side view, in
6 section, taken along section lines 8-8 of FIG. 2, of a
7 silicon substrate 10 at another step in processing, in
8 accordance with an embodiment of the instant invention. A
9 conventional thermal oxidation has been used to provide a
10 silicon dioxide layer 15' on all exposed silicon surfaces
11 and to convert the suspended lattice 18 to silicon dioxide
12 15. As a result of the oxidation, the openings 20 have a
13 reduced width. In one embodiment, the openings 20 have a
14 width of about 1.16 microns and the silicon dioxide
15 separating the openings 20 has a width of about .44 microns.
16 In one embodiment, the oxide 15' has a thickness of about
17 .22 microns. In one embodiment, the oxides 15 and 15' are
18 conventional silicon oxynitride layers.

19
20 FIG. 8 is a simplified side view, in section, taken
21 along section lines 8-8 of FIG. 2, of a silicon substrate 10
22 at another step in processing, in accordance with an
23 embodiment of the instant invention. A layer 55 has been
24 formed to fill all or most of the openings 20. The layer 55

1 may seal the openings 20 and isolate the cavity 200 from
2 potential contamination. The layer 55 may be formed using
3 CVD or gas deposition techniques.

4
5 In one embodiment, a conventional TEOS process may be
6 used to deposit an oxide layer 55. It will be appreciated
7 that formation of the layer 55 may result in some deposition
8 of silicon dioxide within the cavity 200, however,
9 significant improvements in relative dielectric constant and
10 in parasitic capacitance to the substrate may still be
11 provided. Conventional TEOS processes include heating of
12 the substrate 10 in a partial vacuum, resulting in a partial
13 vacuum or gaseous dielectric in the cavity 200 after the
14 TEOS layer 55 seals the openings 20.

15
16 In one embodiment, the oxide layer 55 has been formed
17 to a thickness of about 1.1 microns. The TEOS oxide layer
18 55 is formed and seals the cavity 200, resulting in a
19 continuous oxide layer 55 at and slightly beneath the
20 surface of the silicon substrate 10, filling tops of the
21 cavities 21 and sealing them. In one embodiment, the cavity
22 200 includes a gaseous dielectric.

23

1 FIG. 9 is a simplified side view, in section, taken
2 along section lines 8-8 of FIG. 2, of a silicon substrate 10
3 at another step in processing, in accordance with an
4 embodiment of the instant invention. A conventional
5 chemical-mechanical polish has been used to provide
6 planarized regions 56 on the top surface of the silicon
7 substrate 10 and to remove some or most of the TEOS oxide
8 layer 55 from the regions 11 that will be employed in
9 subsequent processing to provide active electronic
10 components, as discussed above.

11
12 As a result, the planarized region 56 completes a
13 dielectric platform that includes a cavity 200 in the
14 conductive silicon substrate 10. The dielectric constant of
15 the composite structure is greatly reduced compared to,
16 e.g., what would be provided by a thick, predominantly solid
17 dielectric layer. Additionally, reduced stress is induced
18 in the silicon substrate 10 compared to thick dielectric
19 layers or to dielectric layers prepared using etched
20 trenches followed by oxidation, because the dielectric
21 platform does not include long portions formed from oxide
22 and does include substantial volumes that are not occupied
23 by solids having thermal coefficients of expansion differing
24 from that of the silicon substrate 10.

25

1 In one embodiment, the dielectric platform includes
2 voids occupying in excess of 40% of the total volume prior
3 to TEOS deposition. This results in an effective dielectric
4 constant reduction of about 30%, from an ϵ_R of about 3.9 to
5 an effective ϵ_R of about 2.74. In one embodiment, the
6 dielectric platform includes voids occupying in excess of
7 50% of the total volume prior to TEOS deposition. This
8 results in an effective dielectric constant reduction of
9 about 39%, from an ϵ_R of about 3.9 to an effective ϵ_R of
10 about 2.39. Formation of cavity 200 results in further
11 reductions of the effective dielectric constant. In one
12 embodiment, assuming a depth of about three microns for the
13 silicon dioxide lattice 18 and a depth of about five microns
14 for the cavity 200, an effective dielectric constant ϵ_R of
15 about 1.81 is provided over a depth of about 8 microns. As
16 a result, passive elements formed on top of the layer 56 of
17 the dielectric platform 12 have sharply reduced parasitic
18 capacitances to the substrate 10.

19
20 Traditional integrated circuits employ relative thin
21 (e.g., less than one micron) dielectric layers for isolation
22 of passive components and busses from the substrate. In
23 comparison, the dielectric platform 12 of the present
24 invention is capable of providing a substantially thicker

1 dielectric. Additionally, the dielectric platform 12 may be
2 formed to have a reduced dielectric constant relative to
3 conventional dielectric layers. As a result, the effective
4 dielectric constant of the dielectric platform 12 is reduced
5 by both the reduced effective dielectric constant and the
6 increased thickness. In one embodiment, the effective
7 dielectric constant for capacitance between passive
8 components formed on the surface 56 of the dielectric
9 platform 12 and the substrate 10 is reduced by a factor of
10 between one and two orders of magnitude over that of
11 conventional dielectric layers. As a result, parasitic
12 capacitance to the substrate is greatly reduced and losses
13 due to substrate resistance are also dramatically reduced.
14 The amount of current needed to switch the electrical state
15 of conductors formed on the dielectric platform 12 is also
16 dramatically reduced, reducing power requirements for
17 integrated circuits formed using the dielectric platform 12.

18
19 For example, conventional CMOS and bipolar integrated
20 circuits may be formed in areas adjacent to the dielectric
21 platform 12, and these circuits may be coupled to and employ
22 passive components such as spiral inductors, microstrip
23 transmission lines and the like that are formed on the
24 planar surface of the dielectric platform 12. Separating

1 the planar surface from the silicon substrate 10 allows
2 higher Qs to be realized for these passive components.

3

4 FIG. 10 is a simplified and enlarged plan view of a
5 portion the dielectric platform 12 shown in FIG. 1, in
6 accordance with an embodiment of the instant invention. The
7 dielectric platform 12 of FIG. 10 differs from that of FIG.
8 2 et seq. in that the initial masking layer does not include
9 provision for formation of the one or more pillars 17 that
10 were formed within the cavity 200 beneath the region 7. In
11 other words, within the boundary 9 of region 12, the mask 13
12 is formed as described above, but the mask 13 comprises
13 contiguous openings 20 spanning an interior of the mask 13.

14

15 FIG. 11 is a simplified side view, in section, taken
16 along section lines 11-11 of FIG. 10, in accordance with an
17 embodiment of the instant invention. FIG. 11 shows a series
18 of cavities 21 formed by etching the silicon substrate 10
19 through the mask 13 of FIG. 10. In one embodiment, the
20 cavities 21 are etched to a depth of fifteen microns. In
21 one embodiment, the cavities 21 are formed to have a depth
22 of between ten and thirty microns. Sidewalls and bottoms of
23 the cavities have been oxidized to form an oxide layer 15.
24 In one embodiment, the sidewalls have been completely

1 oxidized and a bottom oxide having a thickness of about 0.3
2 microns has been formed. In one embodiment, the sidewalls
3
4 have been completely oxidized and a bottom oxide having a
5 thickness of about one micron has been formed.

6
7 A layer analogous to the layer 55 of FIG. 8 has been
8 formed to seal the openings 20 and to isolate the cavities
9 21 from potential contamination. This layer has been
10 planarized as described with reference to FIG. 9 to form a
11 planarized region 56 sealing the cavities 21.

12
13 FIG. 12 is a simplified plan view of a semiconductor
14 die 60 including passive components 62, 64 and 66 formed on
15 dielectric platforms 12 and transistors 68 formed in the
16 region 11, in accordance with an embodiment of the instant
17 invention. As shown in FIG. 12, the transistors 68 may be
18 MOS devices or bipolar devices. It will be appreciated that
19 other kinds of transistors, diodes and components may also
20 be formed on the semiconductor die 60 using conventional
21 techniques.

22 FIGS. 13A-13D are simplified side views, in section,
23 taken along second lines 33-33 of FIG. 12, in accordance
24 with embodiments of the instant invention. FIG. 13A shows a

1 protective layer 70 formed on a back surface of the silicon
2 substrate 10. The protective layer 70 typically comprises
3 silicon dioxide and silicon nitride. An opening may be
4 formed in the protective layer 70 beneath one or more of the
5 dielectric platforms 11.

6

7 FIG. 13B shows a cavity 76 etched into the substrate 10
8 using the protective layer 70 as an etch mask to define the
9 cavity 76. Etching of the cavity 76 in the silicon
10 substrate 10 may be done using etchants as described in U.S.
11 Patent No. 5,207,866, entitled "Anisotropic Single Crystal
12 Silicon Etching Solution And Method", issued to Ping-Chang
13 Lue and Henry G. Hughes, which is incorporated herein by
14 reference for teachings relating to etching of silicon.
15 Etches prepared in accordance with such techniques may be
16 used to form cavities that are substantially trapezoidal in
17 cross-section and are bilaterally symmetrical about a
18 vertical axis as shown in FIGs. 13B-D. In one embodiment,
19 the larger interior angles of the trapezoidal cross-section
20 are about 54.73 degrees.

21

1 FIG. 13C shows cavity 74 having a recessed region
2 forming a cavity 76 formed by patterning and etching of a
3 second opening in the protective layer 70. The cavity 76
4 results from the combination of the first and second etching
5 steps. The cavity 76 is formed to extend nearly to the
6 oxide layer 15 formed on bottoms of the cavities 21 of FIG.
7 11. In one embodiment, the cavity 76 is formed to stop on a
8 buried epitaxial layer that was previously formed in the
9 silicon substrate 10 using known techniques. The cavity 74
10 is formed to have known dimensions and to be aligned with
11 respect to circuitry formed on the silicon substrate 10.
12 Ridges 78 of silicon delineate edges of the cavity 74.

13
14 FIG. 13D shows the cavities 74 and 76 following
15 stripping of the protective layer 70 and an anisotropic
16 silicon etch that exposes bottoms of the dielectric platform
17 12. The anisotropic silicon etch also removes silicon
18 material from the cavity 74 and from bottoms and sides of
19 the ridges 78.

20
21 FIG. 13E shows the formation of bonding layer 79 on
22 the surfaces of ridges 78 and cavity 74.

23
24 In one embodiment, a thin layer of platinum may be
25 applied to the cavities 74 and 76 and then alloyed to form

1 PtSi in areas where the platinum is in direct contact with
2 silicon material. Excess platinum formed on silicon
3 dioxide, e.g., bottoms of the dielectric platforms 12, may
4 be then removed using conventional techniques such as aqua
5 regia. The silicide is then plated with metals such as
6 titanium, tin, and gold layers or the like.

7

8 In one embodiment, photoresist is deposited in cavity
9 76. Following deposition of a metal layer using conventional
10 techniques, the metal layer is removed from the region of
11 the cavity 76 to provide a dielectric platform 12 that does
12 not have metal plating on a lower surface of the dielectric
13 platform.

14

15 FIG. 14 is a simplified plan view of two semiconductor
16 die 80 and 82 co-located on a common mount 84, in accordance
17 with embodiments of the instant invention. The die 80 is
18 shown to include multiple dielectric platforms 12 such as
19 those illustrated and discussed with respect to FIGs. 10 and
20 11 having passive components 62, 64 and 66, which may
21 include inductors, resistors and/or capacitors formed
22 thereon. Both die 80 and 82 are illustrated as including
23 active components such as transistors 68. The die 80 and 82
24 may be of different types, e.g., an RF chip 80 and a
25 microprocessor 82. Other types of integrated circuit die 82

1 known in the art may be employed as well. The die 80 and 82
2 also include contact pads 86.

3

4 Contact pads 86 typically are formed for a variety of
5 reasons: to allow electrical contact to be made through one
6 or more dielectric layers to other metallization or
7 semiconductive regions on the die 80, 82; to facilitate
8 electrical testing during processing using probes; and to
9 facilitate interconnection of the die 80, 82 to other
10 electronic components.

11

12 It will be appreciated that while only two die 80 and
13 82 are shown in FIG. 14 for simplicity of illustration and
14 ease of understanding, more or fewer die may be mounted on
15 the mount 84.

16

17 FIGs. 15A-15F are simplified side views, in section,
18 taken along section lines 15-15 of FIG. 14, in accordance
19 with embodiments of the instant invention.

20

21 FIG. 15A is a simplified side view of a mount 84
22 comprising a dielectric body 87 and a conductive surface
23 layer 88. The mount 84 also includes elevated regions,
24 appurtenances or pedestals 90 intended to facilitate
25 alignment of the die 80, 82 and also for die attachment.

1 In one embodiment, die attachment is carried out using
2 conventional alloy preforms and thereby forming
3 metallurgical bonds between the silicon substrate 10 and the
4 conductive surface layer 88. In one embodiment, the
5 dielectric body 87 comprises ceramic. In one embodiment,
6 the dielectric body 87 comprises beryllia. In one
7 embodiment, the dielectric body 87 comprises a material
8 chosen from a group consisting of alumina, alluminum
9 nitride, and other suitable ceramic materials.

10

11 The material forming the dielectric body 87 is chosen
12 to provide the desired bonding characteristics for the
13 conductive layer 88, ability to withstand thermal and other
14 subsequent treatments, ability to provide heatsinking
15 capability for the die 80, 82 and ability to provide
16 adequate mechanical support, including appropriate thermal
17 coefficient of expansion matching, for the die 80, 82. In
18 one embodiment, the conductive layer may include materials
19 chosen of titanium nichol gold, or the like. In one
20 embodiment, the conductive layer 88 extends beneath the
21 dielectric platforms 12.

22

23 FIG. 15B is a simplified side view similar to that of
24 FIG. 15A, however, the conductive layer 88 has been

1 patterned so that it does not extend beneath the dielectric
2 platform 12 that has had silicon removed from beneath it.
3 This allows passive component 62 (FIG. 14) to produce fields
4 which penetrate dielectric platform 12, cavity 76, and into
5 dielectric material 87 of mount 84. As compared to FIG 15A,
6 where conductive layer 88 prevents penetration of fields
7 into dielectric region 87 of mount 84.

8

9 The pedestals 90 are designed to fulfill several
10 different functions. A thickness of the ridges 78 is known
11 a priori. Additionally, spatial relationships between the
12 ridges 78, the cavities 76 and passive 62, 64, 66 and active
13 68 circuitry are known a priori. Further, by ensuring
14 mutual planarity of the pedestals 90, it is possible to
15 mount the die 80, 82 so that top surfaces of the die 80, 82
16 are substantially co-planar and so that relative positions
17 of passive 62, 64, 66 and active 68 components formed on
18 each of the die 80, 82 are predetermined with a degree of
19 accuracy sufficient to allow later formation of
20 interconnections therebetween. Thicknesses of the pedestals
21 90 are chosen to exceed the thickness of ridges 78 so that
22 the die 80, 82 are supported and bonded by planar portions
23 89 of the cavities 74, rather than by the ridges 78. Areas
24 of the pedestals 90 are chosen to be slightly smaller than

1 areas of the cavities 74 in order that positioning the die
2 80, 82 on the pedestals results in placement of the die 80,
3 82 relative to each other and the mount 84 to a
4 predetermined degree of accuracy.

5

6 FIG. 15C is a simplified side view of an embodiment of
7 the mount 84 and two die 80, 82 mounted thereon, in
8 accordance with an embodiment of the instant invention. In
9 one embodiment, the mount 84 is formed from a conductive
10 material. In one embodiment, the mount 84 is formed from
11 metal. In one embodiment, the mount 84 is formed from a
12 material chosen from a group consisting of copper, copper
13 tungsten alloy, kovar, molybdenum, and the like, having
14 good thermal conductivity, and matching the thermal
15 coefficient of expansion of silicon.

16

17 FIG. 15D is a simplified side view of an embodiment of
18 the mount 84 and two die 80, 82 mounted thereon, in
19 accordance with an embodiment of the instant invention. The
20 mount 84 is formed from a conductive material but includes
21 an opening 92 formed in a top surface of the pedestal 90
22 configured to provide an increased separation from passive
23 component 62. This allows passive component 62 (FIG. 14) to
24 produce fields which penetrate dielectric platform 12,

1 cavity 76, and into dielectric cavity 92. As a result,
2 parasitic capacitance to ground is reduced compared to the
3 configurations illustrated in FIG. 15C. In one embodiment,
4 the opening 92 is formed to have a depth of about 50 to 500
5 microns. In one embodiment the depth of dielectric cavity
6 92 is about 100 microns.

7

8 In one embodiment, the pedestal is formed to have a
9 height that is slightly greater than a depth of the cavity
10 74 formed in the die 80. In one embodiment, the pedestal
11 comprises a bilaterally symmetrical trapezoidal cross
12 section and wherein the smallest angles in the cross section
13 are about 54.73 degrees.

14

15 FIG. 15E is a simplified side view of the mount 84
16 according to any of the embodiments of the invention, having
17 two die 80, 82 mounted thereon, and further including a ring
18 of material 94. In one embodiment, the ring of material 94
19 is formed from a dielectric material. In one embodiment,
20 the ring of material surrounds the die 80, 82 on all lateral
21 edges. In one embodiment, the material 94 does not form a
22 ring and abuts selected portions of the die 80, 82. In one
23 embodiment, the material 94 is formed on the mount 84 before
24 placement and bonding of the die 80, 82. In one embodiment,

1 the material 94 is coupled to the mount 84 after attachment
2 of the die 80,82 to the mount 84. The material 94 is
3 configured to abut the die 80, 82 with a predetermined
4 separation from the die 80,82 and to have an upper surface
5 that is substantially coplanar with upper surfaces of the
6 die 80, 82. Material 94 may be comprised of the same
7 materials as listed as options for material 87 of
8 FIG. 15A-B.

9

10 FIG. 15F is a simplified side view of the mount 84,
11 the die 80, 82 mounted thereon and the material 94 following
12 application and (if needed) planarization of a dielectric
13 layer 96. The dielectric layer 96 occupies interstices
14 between the die 80, 82, between the die 80, 82 and the
15 material 94 and also may extend across top surfaces of the
16 die 80, 82. The dielectric layer 96 is chosen to provide an
17 appropriate thermal coefficient of expansion match to the
18 mount 84 and die 80, 82, to provide planar surfaces bridging
19 interstices between die 80,82 and between die 80 or 82 and
20 the material 94, to insulate various elements from one
21 another and to permit patterning of the dielectric layer 96.

22

23 Fig. 16 shows mount 84 in further detail. A passive
24 component 62 is disposed on an upper surface of
25 planarization layer 96. Passive component 62 generates a

1 field 75 which penetrates dielectric layer 96 and dielectric
2 platform 12 to impinge on dielectric cavity 76 and
3 dielectric cavity 92. It should be appreciated that a
4 number of types of electrical components may be used to
5 generate field 75. In one embodiment, passive component 62
6 operates as an inductor generating field 75 as a magnetic
7 field. In one embodiment, passive component 62 produces an
8 electric field that penetrates cavity 92.

9

10 Fig. 17 shows a simplified plan view of two die 80, 82
11 mounted on a mount 84 together with dielectric material ring
12 94. Regions between the die 80 and 82 and between the die
13 80, 82 and the dielectric material ring 94 have been filled
14 with a planarized dielectric layer 96 having a surface that
15 is coplanar with or parallel to surfaces of the die 80 and
16 82, and dielectric material ring 94. Vias 100 have been
17 formed through the dielectric layer 96, allowing
18 interconnections 98 to be formed on the die 80, 82 to some
19 of the pads 86 associated with the transistors 68 and the
20 passive components 62-66. The interconnections 98 also
21 couple signals between the two die 80, 82 and between the
22 two die 80 and 82 and the mount 84. An exemplary material
23 for the dielectric layer 96 is epoxy. Another exemplary
24 material for the dielectric layer 96 is polyamide.

1 Dielectric layer 96 material can be comprised of polyamide,
2 low temperature deposited glass, dielectric epoxy, a
3 combination of the two or more, or the like.

4

5 The interconnections 98 may be formed using
6 conventional techniques and may use geometries that are
7 larger than those typically used in forming integrated
8 circuit die. An example is described in U.S. patent No.
9 5478773, entitled "METHOD OF MAKING AN ELECTRONIC DEVICE
10 HAVING AN INTEGRATED INDUCTOR", issued to Stephen Dow, Eric
11 C. Mass, and Bill Marlin, which is incorporated herein by
12 reference for teachings relating to the present invention.
13 In some embodiments, the passive components 62-66 are also
14 formed together with the interconnections 98. In one
15 embodiment, the interconnections 98 are formed from
16 electroplated or electroless gold, or the like, having a
17 thickness of in excess of one micron, using known
18 techniques. Interconnection metal 98 can also be used to
19 form inductor component 62 resulting in an inductor
20 having higher Q than is provided by interconnect layers
21 associated with the typical fabrication of IC die 80, 82.

22

23 Further processing of the assembly shown in FIG. 17,
24 such as encapsulation or capping to passivate or seal in
25 circuitry and interconnect metalization between die 80, 82

1 and metalized regions 88 of dielectric material ring 94,
2 should be considered as a completion of the fabrication of
3 the resulting thick film device.

4

5 The foregoing detailed description of the instant
6 invention for the purposes of explanation have been
7 particularly directed toward formation of a dielectric
8 platform allowing high Q inductors to be formed on silicon
9 wafers together with transistors and other microelectronic
10 components, and a precision coplanar alignment of more than
11 one die and surrounding coplanar dielectric materials on a
12 common mount.

13

14 It will be appreciated that the need for thick,
15 monolithic dielectric films has been described along with
16 methods for meeting that need. A novel low dielectric
17 constant insulator has been described that finds application
18 in RF integrated circuits and in formation of
19 interconnections for high speed digital circuits. The
20 dielectric platform 12 also provides a substantial reduction
21 in noise induced in the substrate 10 and coupled from the
22 substrate 10 to other components due to switching
23 transients. It will be appreciated that improvements in

1 processing techniques may enable formation of dielectric
2 platforms having smaller dimensions and thicknesses than
3 have been described herein without departing from the scope
4 of the appended claims.

5 Various changes and modifications to the embodiment
6 herein chosen for purposes of illustration will readily
7 occur to those skilled in the art. For example, the depth
8 of the openings in the silicon substrate may be chosen as
9 may be desired for a specific application. To the extent
10 that such modifications and variations do not depart from
11 the spirit of the invention, they are intended to be
12 included within the scope thereof which is assessed only by
13 a fair interpretation of the following claims.

14 Having fully described the invention in such clear and
15 concise terms as to enable those skilled in the art to
16 understand and practice the same, the invention claimed is:

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:
 - a die attach surface having a first pedestal;
 - a first semiconductor die having a first surface formed with a first cavity for mounting the first semiconductor die on the first pedestal; and
 - a reactive component disposed on a second surface of the first semiconductor die in a region overlying the first pedestal.
2. The semiconductor device of claim 1, where the reactive component includes an inductor.
3. A semiconductor device, comprising:
 - a first semiconductor die having a first surface formed with a first cavity; and
 - a base; and
 - a first pedestal formed on the base for engaging with the cavity, where the first pedestal has a recessed region for forming a dielectric volume.

4. The semiconductor device of claim 3, further comprising an electrical component disposed on a second surface of the semiconductor die in a region overlying the dielectric volume.

5. The semiconductor device of claim 4, where the electrical component operates as an inductor.

6. The semiconductor device of claim 3, where the dielectric volume comprises a dielectric material.

7. The semiconductor device of claim 6, where the dielectric material is gaseous.

8. The semiconductor device of claim 3, where a surface of the pedestal includes a conductive material for operating as a ground shield of the first semiconductor die.

9. The semiconductor device of claim 3, further comprising:

a second pedestal disposed on the base; and

a second semiconductor die having a first surface formed with a cavity for mounting to the second pedestal.

10. The semiconductor device of claim 9, further comprising a dielectric material disposed between the first semiconductor die and the second semiconductor die.

11. The semiconductor device of claim 9, further comprising a conductor disposed for coupling an electrical signal between the first semiconductor die and the second semiconductor die.

12. A method of operating a semiconductor device, comprising the steps of:

providing a base having a first pedestal for mounting against a first cavity of a first semiconductor die; and

generating a first field with a first electrical component of the semiconductor die, where the first field penetrates a recessed region of the first pedestal.

13. The method of claim 12, where the step of generating includes the step of inducing a magnetic field in the recessed region.

14. The method of claim 12, where the step of generating includes the step of generating the first field in a dielectric material of the recessed region.

15. The method of claim 12, further comprising the steps of:

generating a second field with a second electrical component of the semiconductor die; and

terminating the second electric field on a conductive portion of the pedestal.

16. The method of claim 12, further comprising the steps of:

providing a second pedestal of the base for mounting against a second cavity of a second semiconductor die; and

coupling an electrical signal from the first semiconductor die to the second semiconductor die.

17. An integrated circuit, comprising:
a semiconductor die having a first surface formed with a recession; and
a die attach base having a raised appurtenance for aligning with the recession of the semiconductor die; and
an inductor formed on a second surface of the semiconductor die to overlie a recessed region of the raised appurtenance.

18. A die attach mount comprising;
a base; and

a die attach pedestal configured to engage with a first semiconductor die, where the die attach pedestal has a recessed region for forming a dielectric volume, and the first semiconductor die having a first surface formed with a first cavity configured to engage with the die attach pedestal.

19. The die attach mount of claim 18, wherein the die attach pedestal comprises a bilaterally symmetrical trapezoidal cross-section and wherein the smallest angles in the cross-section are about 54.73 degrees.

20. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar dielectric material forming the base; and

a frustum of a four-sided pyramid having a broad base coupled to the base.

21. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar dielectric material forming the base;

a frustum of a four-sided pyramid having a broad base coupled to the base, a height of the frustum being configured to be slightly less than a depth of a cavity formed in a rear surface of the semiconductor die.

22. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar dielectric material forming the base;

a frustum of a four-sided pyramid forming the pedestal, the pedestal having a broad base coupled to the base; and

a conductive coating formed over some exposed surfaces of the base and the pedestal, wherein no conductive coating is present on regions of the pedestal configured to be placed in proximity to one or more dielectric platforms formed on the first semiconductor die, the dielectric platform having a lower surface extending into the first cavity.

23. The die attach mount of claim 18, wherein the base and the pedestal comprise conductive material.

24. The die attach mount of claim 18, wherein the base and the pedestal comprise:

a generally planar base;

a frustum of a four-sided pyramid formed from conductive material and having a broad base coupled a surface of the generally planar base, a height of the frustum being configured to be slightly less than a depth of a cavity formed in a rear surface of the semiconductor die, the frustum further comprising a small cavity formed on a top surface of the pedestal on regions of the pedestal configured to be placed in proximity to one or more dielectric platforms formed on the first semiconductor die.

25. The die attach mount of claim 18, further comprising a first semiconductor die having a first surface defining a recessed region wherein the pedestal is electrically and mechanically engaged with at least a portion of the recessed region.

26. The die attach mount of claim 18, further comprising a first semiconductor die having a first surface defining a recessed region wherein the pedestal is mechanically engaged with at least a portion of the recessed region.

1 DIE ATTACHMENT AND METHOD

2
3 ABSTRACT OF THE DISCLOSURE

4 A method for forming a semiconductor device including a
5 die attach surface having a first pedestal and a first
6 semiconductor die having a first surface formed with a first
7 cavity for mounting the first semiconductor die on the first
8 pedestal. Further provision is made for the formation of a
9 dielectric cavity in the semiconductor die, the first
10 pedestal or both. The cavity allows for fields produced by
11 electronic components disposed on the upper surface of the
12 semiconductor die to penetrate into the dielectric cavity.

13 Inclusion of a second pedestal on a common die attach
14 surface and a second semiconductor die having second cavity
15 for mounting provides for substantially coplanar precision
16 alignment of the first and second semiconductor die.

FIG. 1 is a schematic diagram of a system for providing a user with a personalized experience. The system includes a user device 10, a server 11, and a database 12. The user device 10 is connected to the server 11 via a network 9. The server 11 is connected to the database 12 via a network 10. The database 12 stores user data and provides it to the server 11, which then provides it to the user device 10.

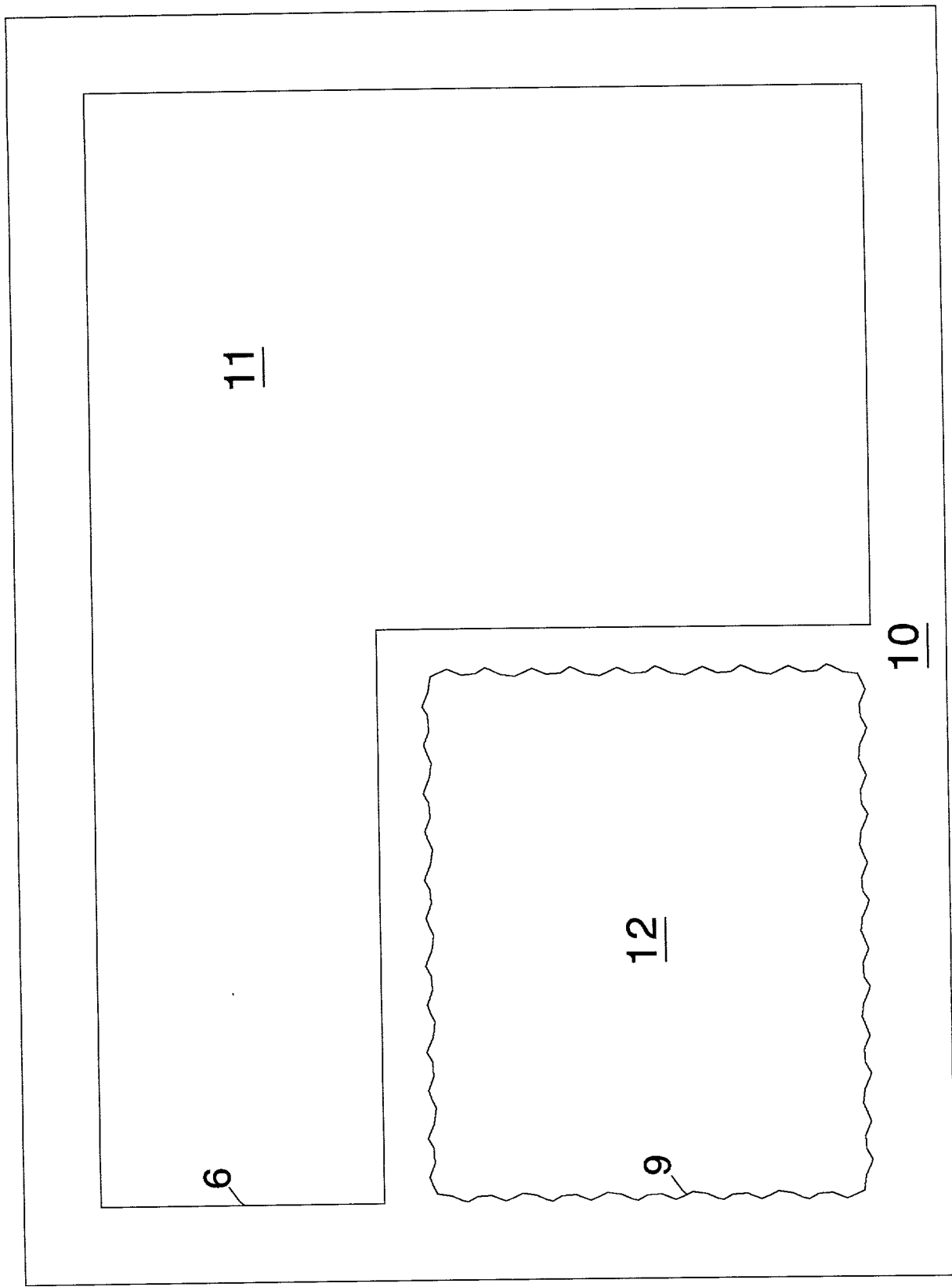


FIG. 1

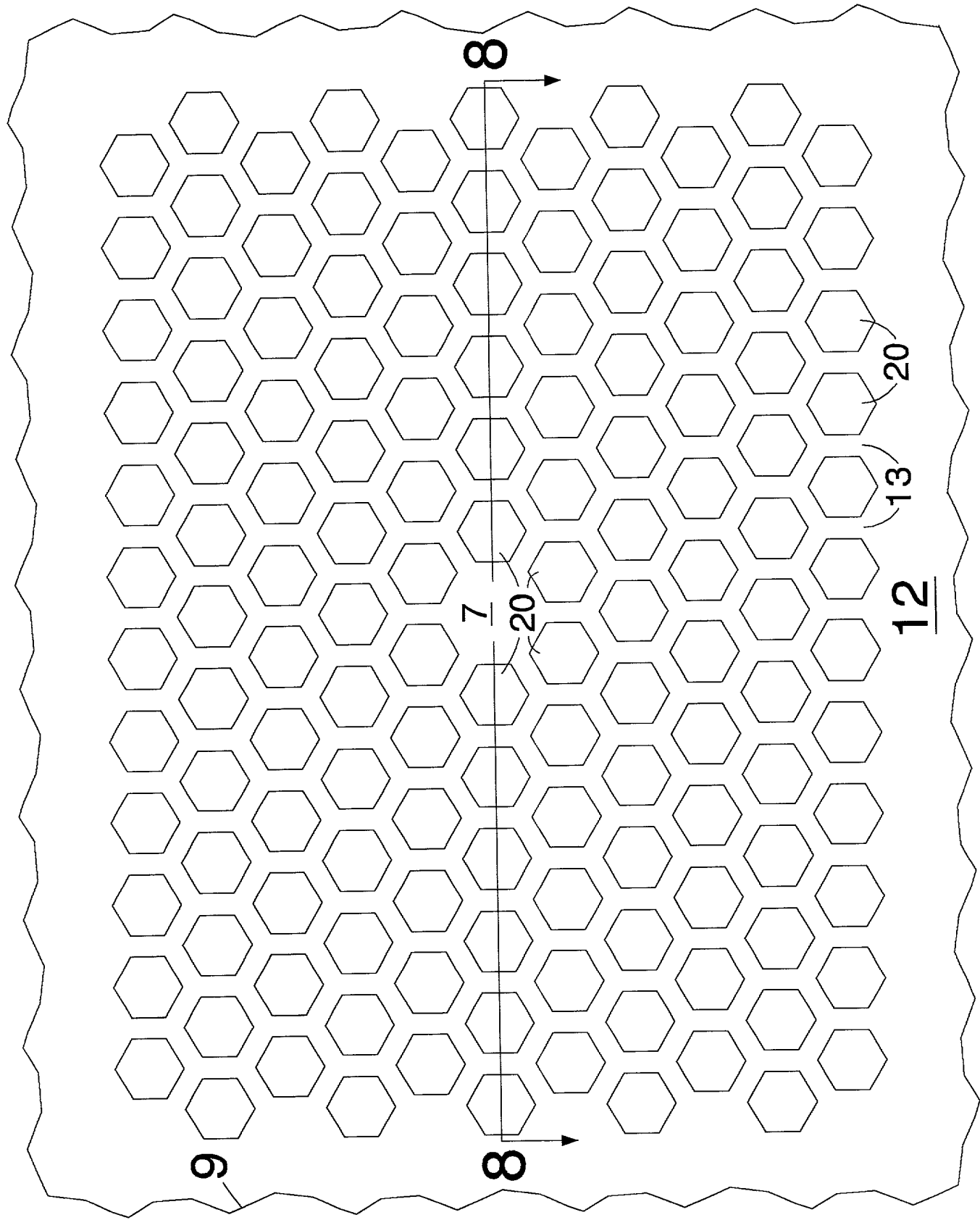


FIG. 2

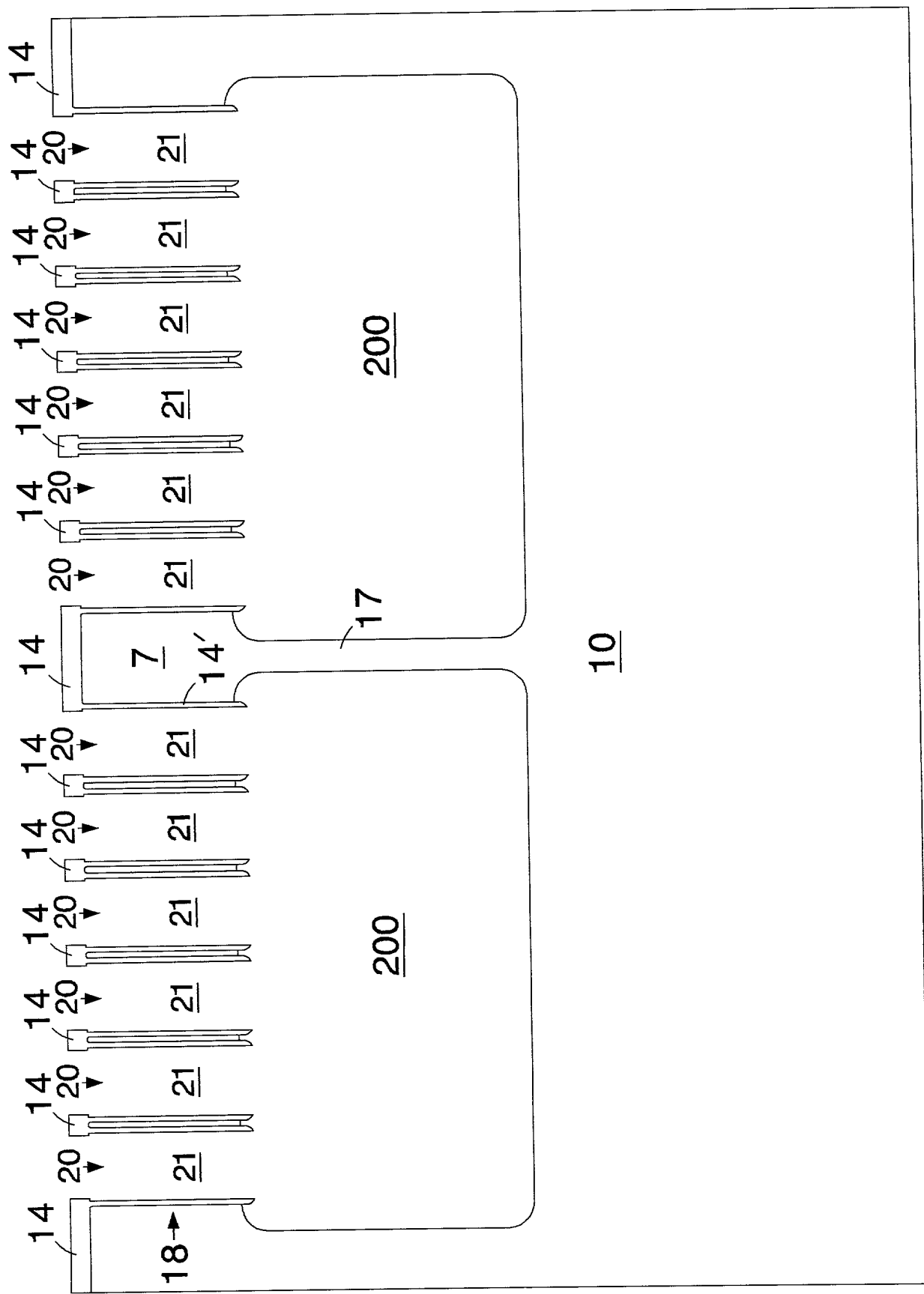


FIG. 6

FIG. 7 is a schematic diagram of a device 10, showing a top view of the device. The device 10 includes a substrate 15, a plurality of conductive lines 20, and a plurality of conductive pads 21. The conductive lines 20 are arranged in a grid pattern, and the conductive pads 21 are arranged in a grid pattern. The device 10 is shown in a perspective view, with the substrate 15 and the conductive lines 20 and pads 21 being visible. The device 10 is shown in a perspective view, with the substrate 15 and the conductive lines 20 and pads 21 being visible.

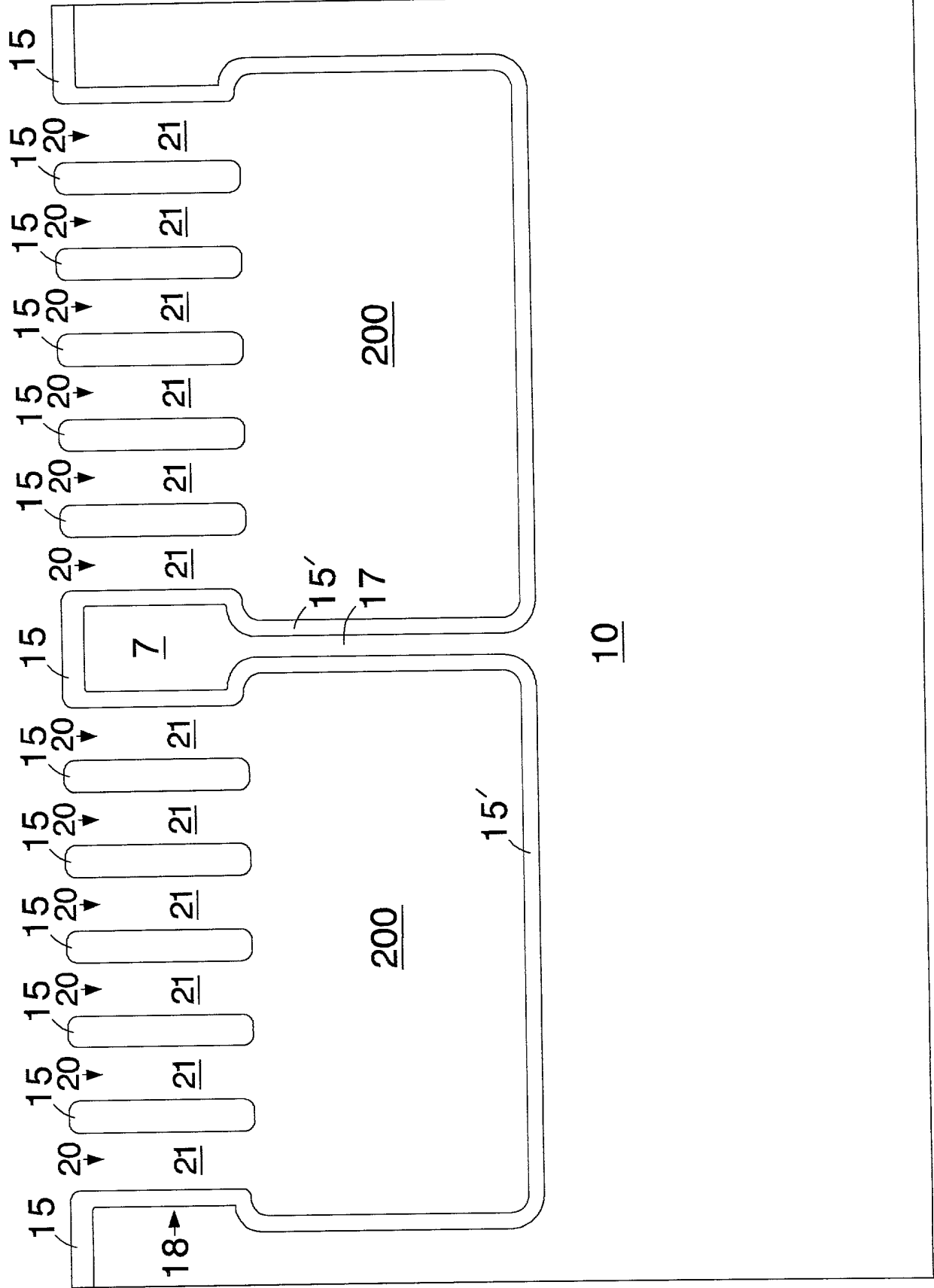


FIG. 7

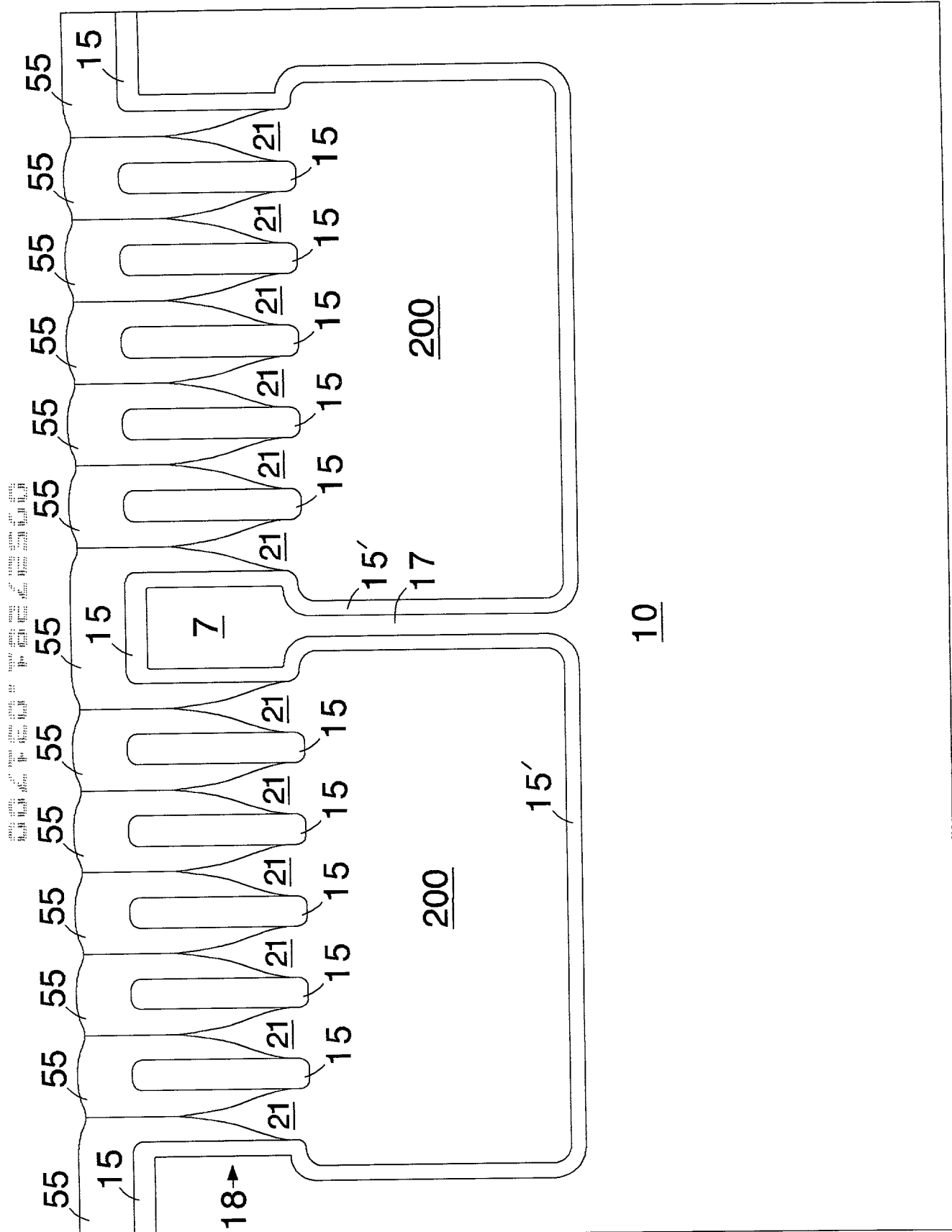


FIG. 8

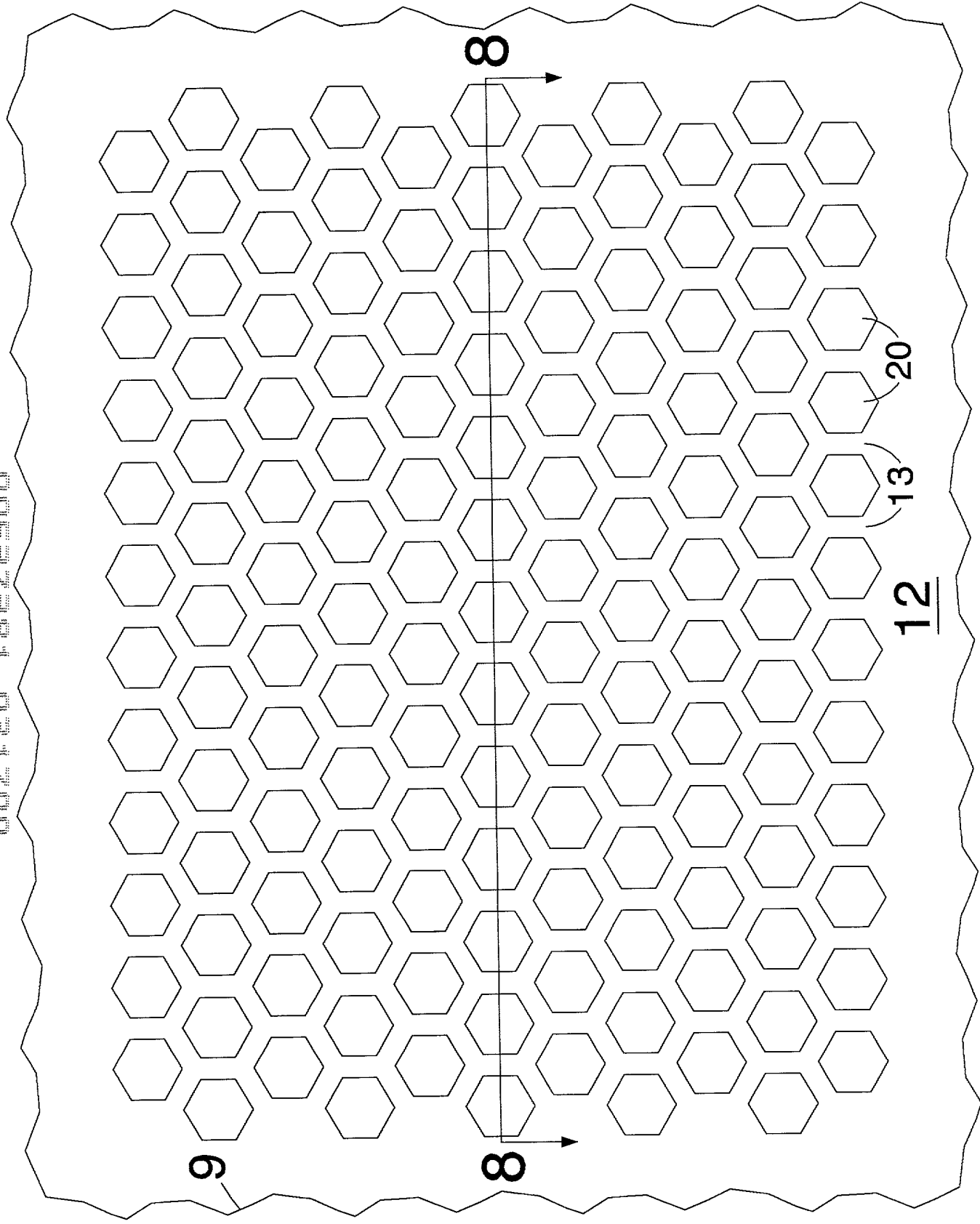


FIG. 10

FIG. 11 is a schematic diagram of a device 10, showing a series of vertical bars 15, each having a top edge 56 and a bottom edge 55. The bars are connected by a horizontal line 21 at the bottom. The device is shown in a perspective view, with the bars 15 and the horizontal line 21 being the main components. The top edge 56 and bottom edge 55 are indicated by dashed lines. The horizontal line 21 is shown as a solid line. The device 10 is shown in a perspective view, with the bars 15 and the horizontal line 21 being the main components. The top edge 56 and bottom edge 55 are indicated by dashed lines. The horizontal line 21 is shown as a solid line.

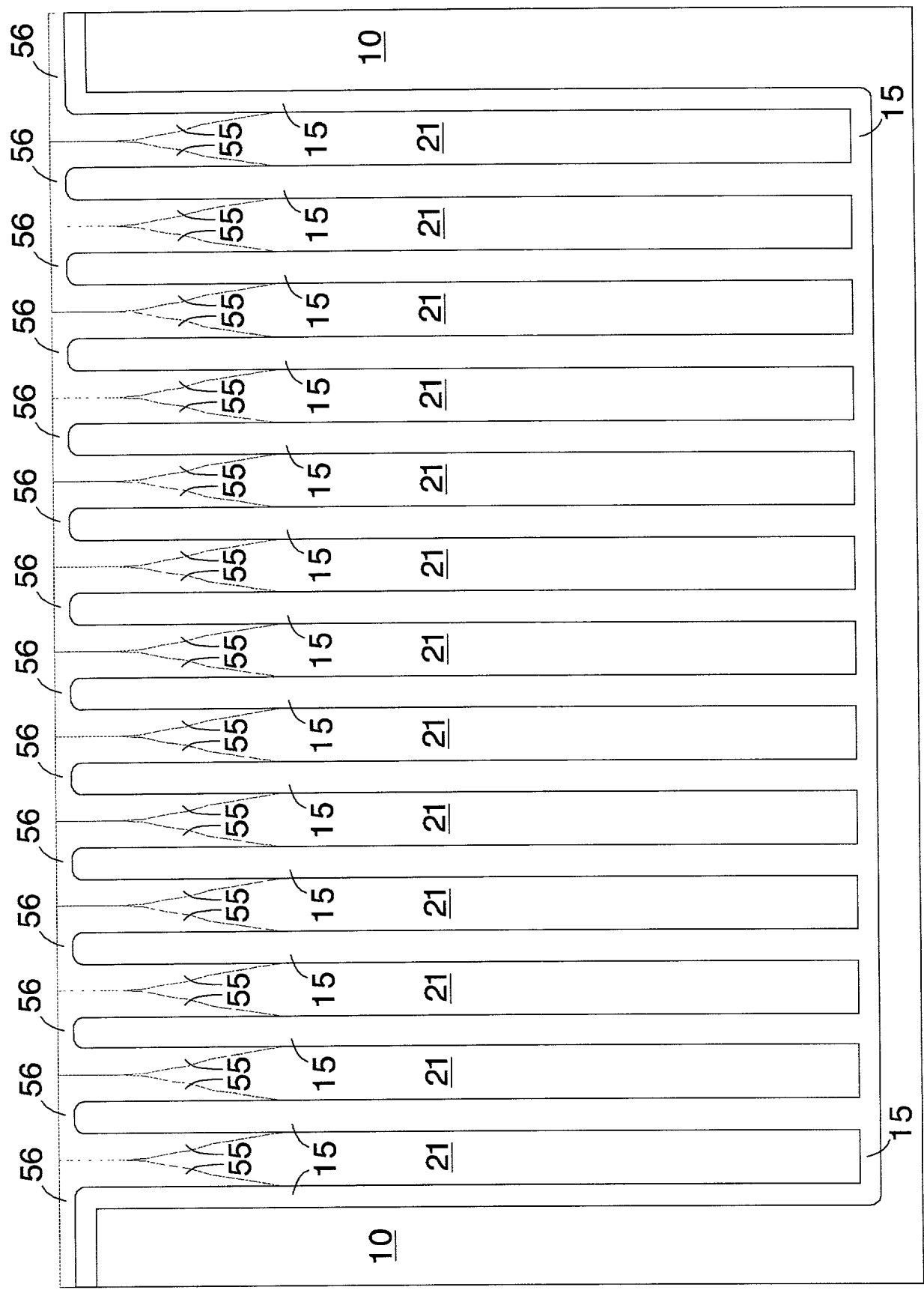


FIG. 11

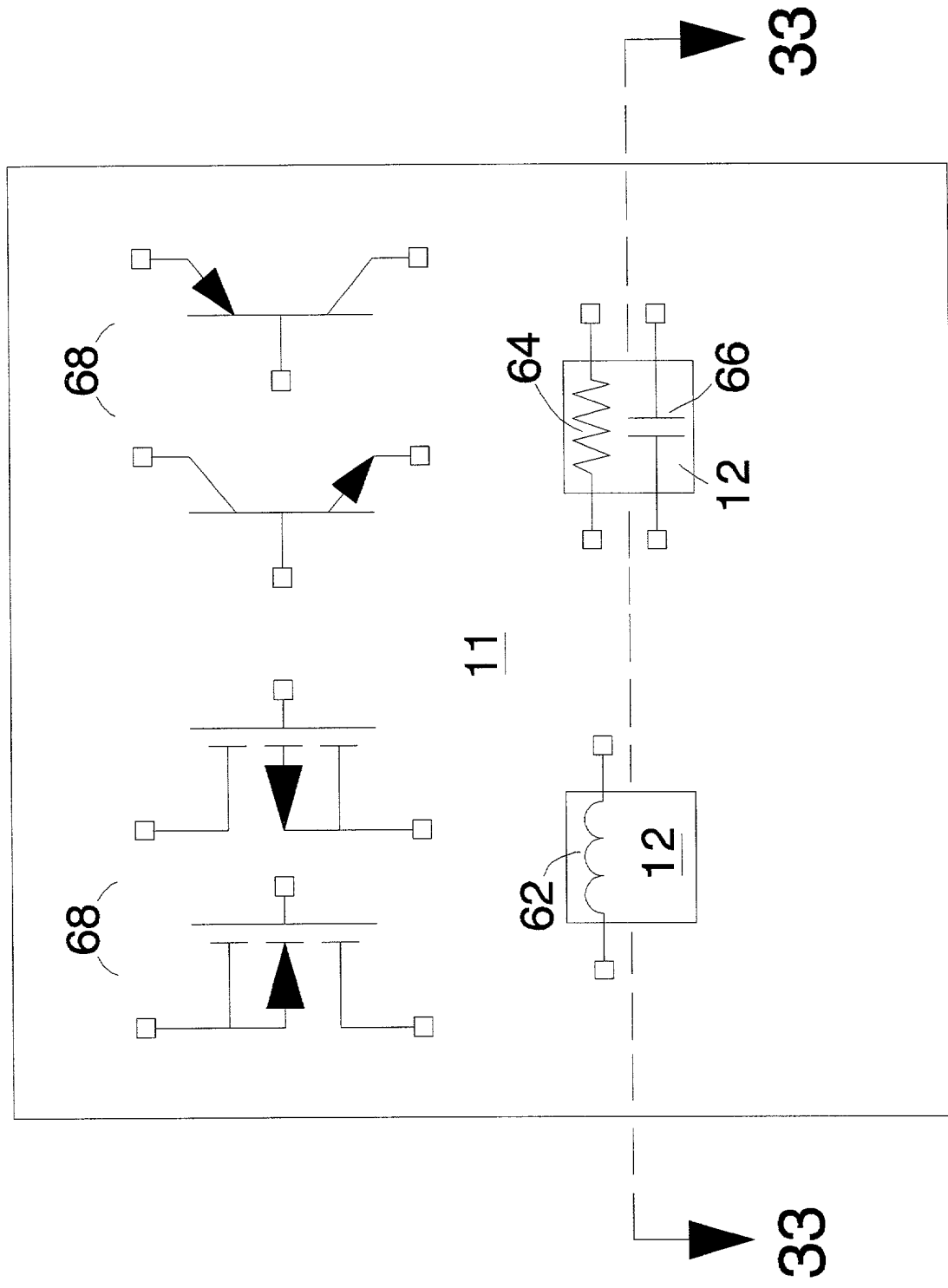


FIG. 12

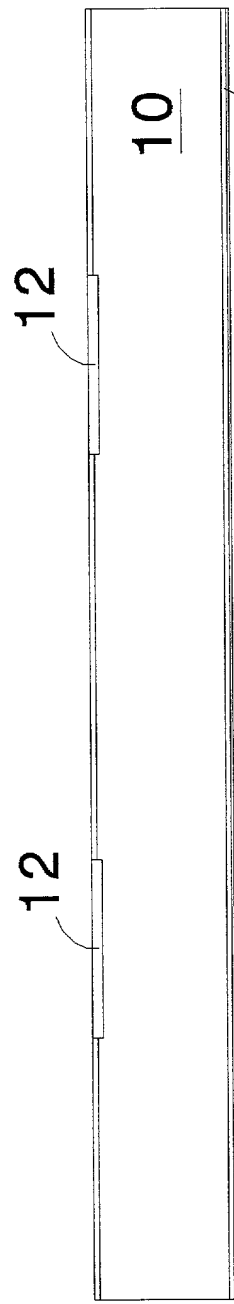


FIG. 13 A

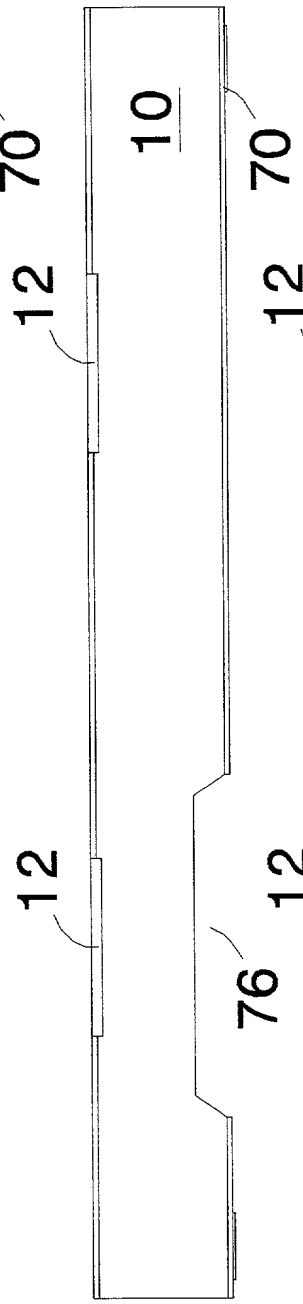


FIG. 13 B

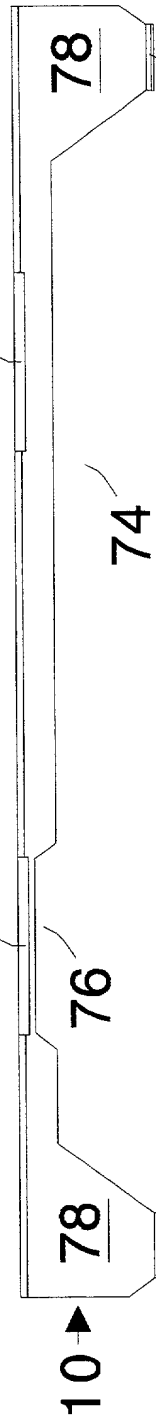


FIG. 13 C

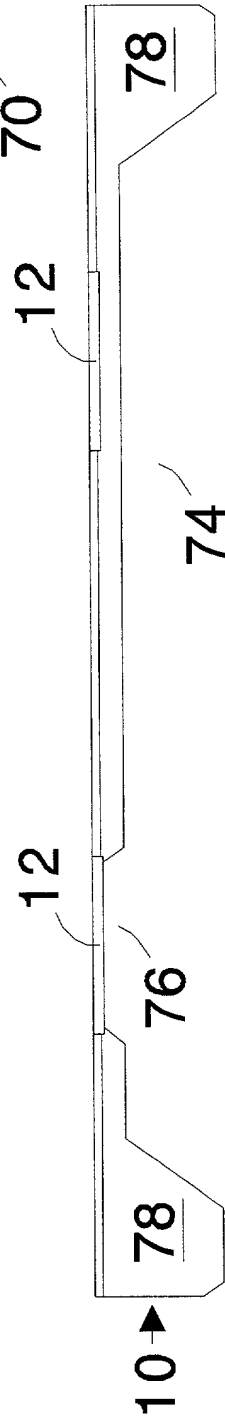


FIG. 13D

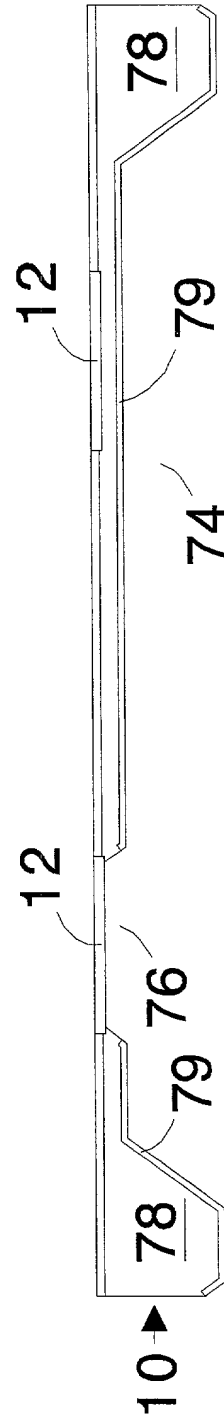


FIG. 13E

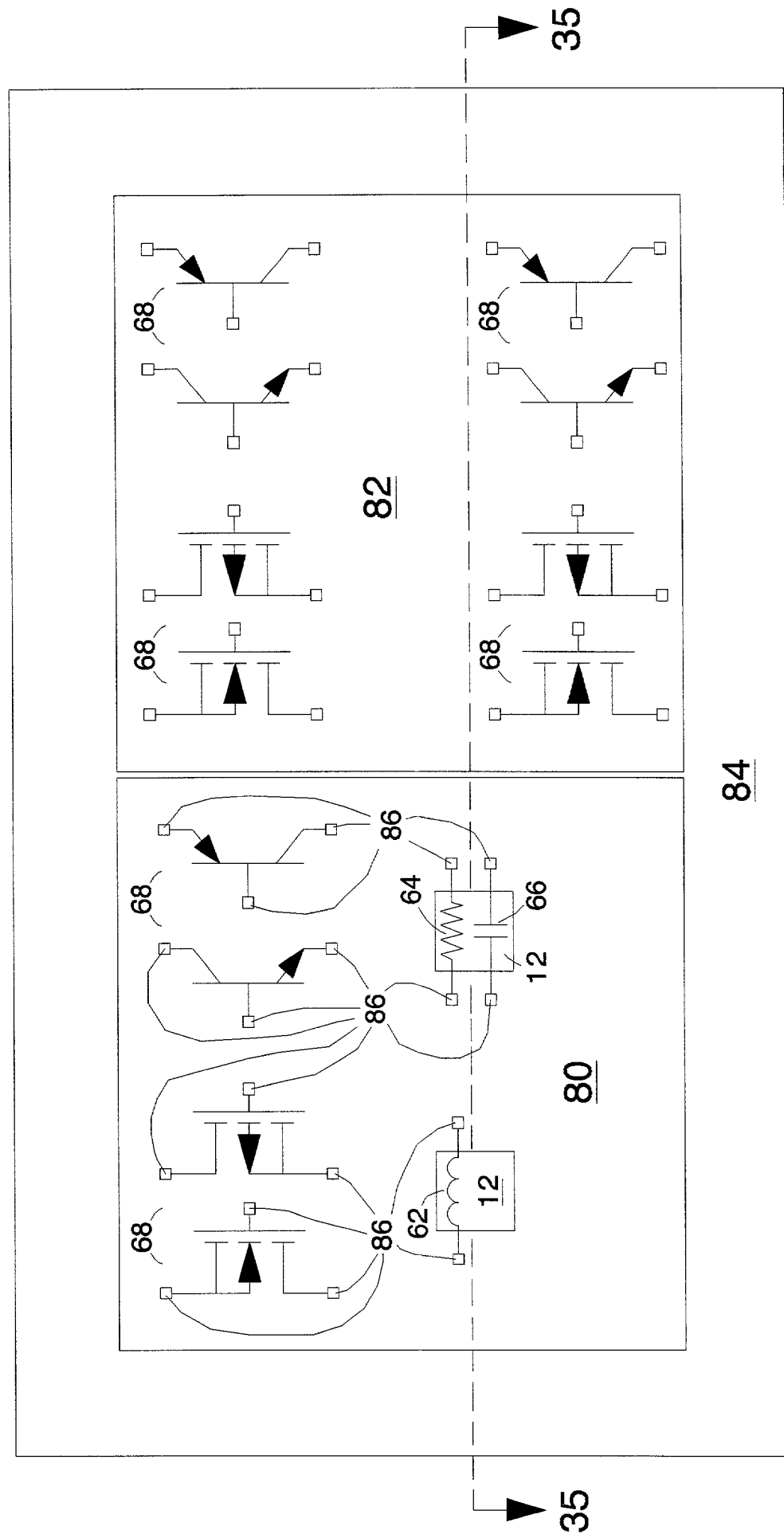
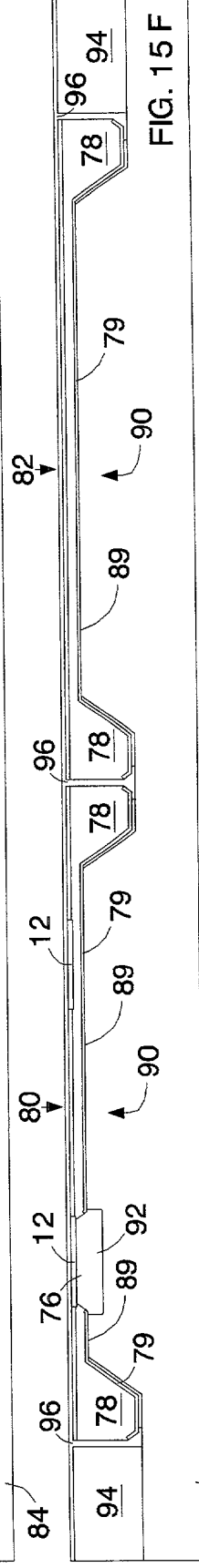
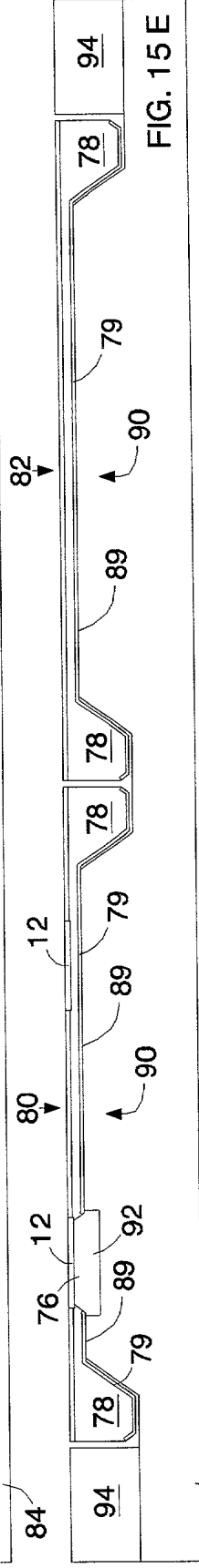
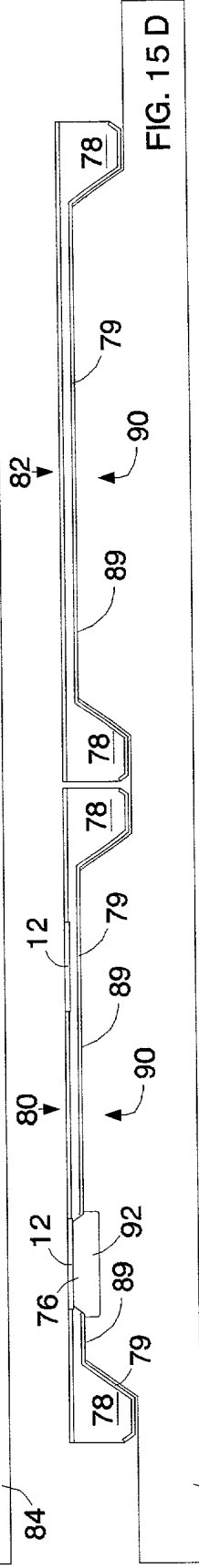
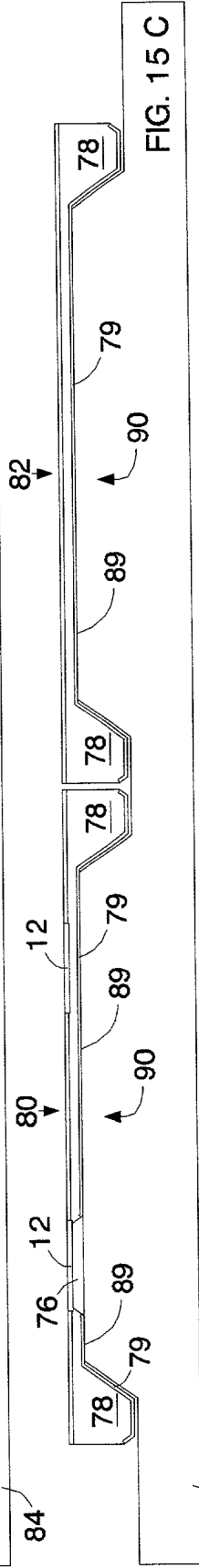
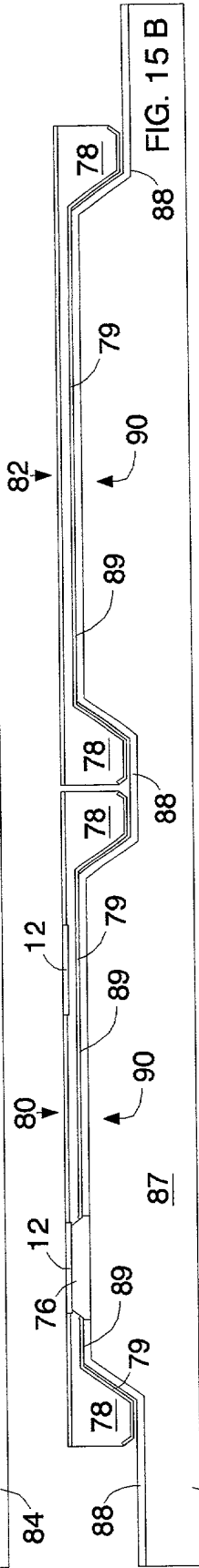
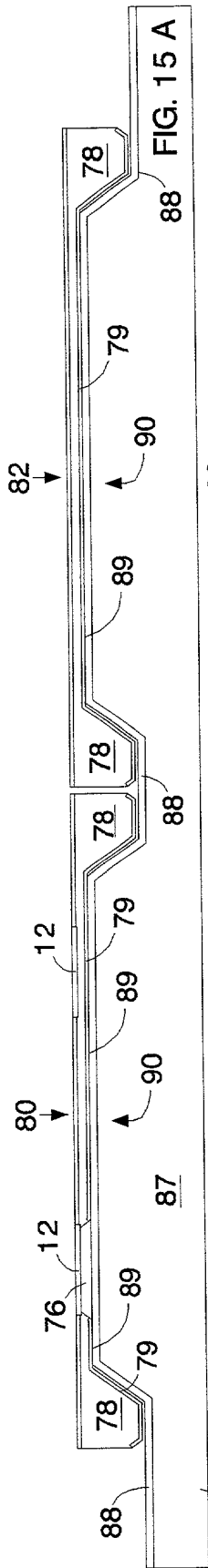


FIG. 14



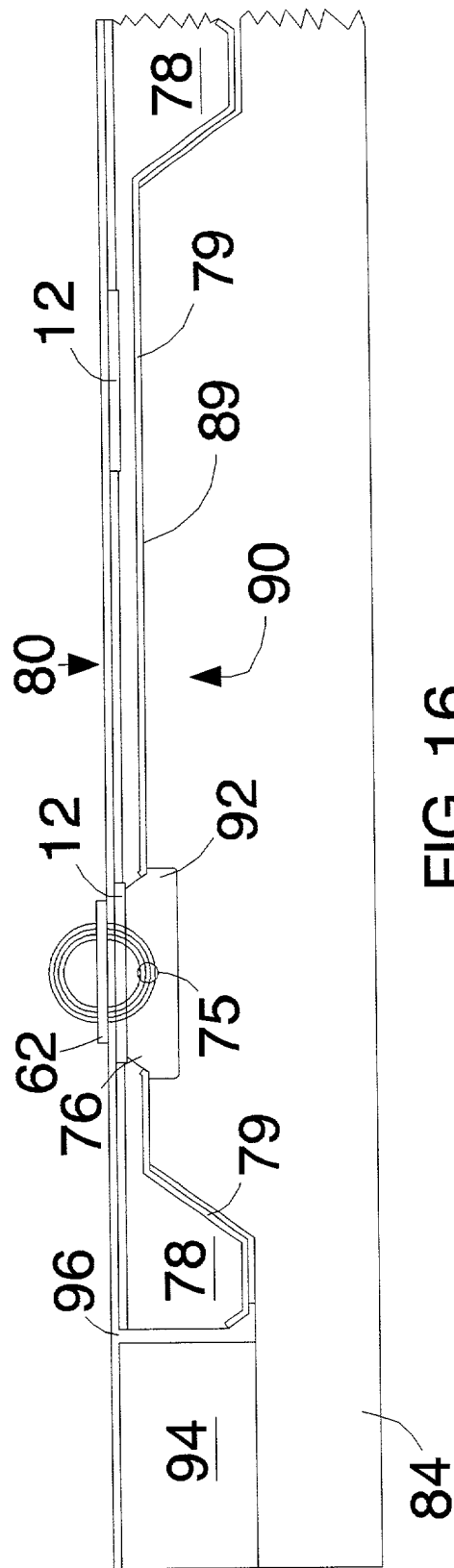


FIG. 16

DECLARATION FOR PATENT APPLICATION

Docket Number RBD-IC-2000

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "DIE ATTACHMENT AND METHOD", the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim the benefit under Title 35, United States Code, § 119(e) of the United States provisional application(s) listed below.

(Application Number)

(Filing Date)

(Application Number)

(Filing Date)

Address all telephone calls to Mr. Robert Davies at telephone no. (480) 945-4950 and address all correspondence to Mr. Robert Davies at 433 E. McKinley, Tempe AZ 85281.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that

these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF FIRST INVENTOR Robert Bruce Davies	INVENTOR'S SIGNATURE <i>Robert Bruce Davies</i>	DATE 17 MAR 2000
RESIDENCE 433 E. McKinley, Tempe AZ 85281	CITIZENSHIP. United States	
POST OFFICE ADDRESS Same as above		